Proceedings of the Ninth IASTED European Conference
Power and Energy Systems (EuroPES 2009)
September 7 - 9, 2009 Palma de Mallorca, Spain

THEORETICAL ANALYSIS OF A FIVE-LEVEL VOLTAGE SOURCE MODULAR INVERTER FOR RENEWABLE ENERGY APPLICATIONS

Grain P. Adam, Olimpo Anaya-Lara and Graeme Burt
Department of Electronic & Electrical Engineering
University of Strathclyde
Royal College Building
204 George St
Glasgow, G1 1XW
Emails: grain.adam@eee.strath.ac.uk[1], olimpo.anaya-lara@eee.strath.ac.uk[2] and g.burt@eee.strath.ac.uk[3]

ABSTRACT
The principle of operation, theoretical basis of pulse width modulation and capacitors voltage balancing method of a five-level modular inverter are presented. Several load scenarios are considered such as operation with different modulation indices, load power factors, imbalance load, symmetrical and asymmetrical faults. In addition, a scenario with utility interface of storage system is considered. Computer simulations in Matlab-Simulink environment are used to validate the operation of the inverter.

KEY WORDS
Cascaded multilevel inverter, diode clamped inverter, modular inverter and sinusoidal pulse width modulation.

1. Introduction

The primary objective of multilevel inverters is to increase their output voltage and power so that they can be applied to high-voltage high-power applications. The main advantages of multilevel inverters are [1]-[4]:

- High quality output voltage at reduced switching frequency.
- Low switching losses and voltage stress on switching devices dv/dt.
- Can operate at high voltage without the need for an interface transformer (reduce construction cost).

However, conventional multilevel inverters suffer from several drawbacks such as: diode clamped multilevel inverters with more than three levels are not able to operate with high load power factors and high modulation indices due to dc link voltage imbalance problem [4]-[12]. Cascaded multilevel inverters require complex and expensive transformer at their inputs for applications that involve real power exchange. This may the increase the construction cost significantly [2].
Capacitor-clamped multilevel inverters with more than three levels require a number of large capacitors, complex capacitors voltage balancing method and are unable to operate in applications that require large amounts of reactive power such as reactive power compensation devices [2],[9].
The modular multilevel inverter proposed in [13]-[14] as potential alternative to conventional multilevel inverters combines all the features of conventional multilevel inverters and provides a number of additional features, such as:

- Modular in construction.
- Extendable to any number of levels; and capacitors voltage balancing is attainable with increased number of levels regardless of the operating conditions.
- Capable of continuous operation with unbalanced load without increasing the risk of system collapse as a result of device failure due to excessive voltage stress.
- Better fault ride through capability.

In [13] the authors use space vector pulse width modulation (SVPWM) to control the modular inverter. However, the use of SVPWM with a modular inverter has no advantage. Especially it will not be able to operate successfully under unbalanced conditions or survive asymmetrical faults, because SVPWM will be invalid during such operating conditions. The capacitors voltage balancing method proposed in [14] has limitations because it requires set points for capacitor voltages to be specified externally.

This paper presents a theoretical analysis of five-level modular inverters, including, principle of operation and capacitor voltage balancing based on carrier based sinusoidal pulse width modulation (SPWM). The main advantages of the proposed method are, it does not require set point for capacitor voltages, instead it distributes the total dc equally across all the capacitors and it can ride through different types of faults, including single-phase open circuit.

2. Modular Multilevel Inverter

2.1 Operational Principle of a Modular Inverter

Fig. 1 shows one cell of a modular multilevel inverter. The switching devices S_m and S_c must be operated in complementary manner. When the switch S_m is turned on S_c is turned off, the voltage across points *a* and *b*, $V_{ab}=0$; when the switch S_m is turned off and S_c is turned on, the voltage produced across points *a* and *b*, $V_{ab}=V_{dc}$. Table 1 summarizes the switch states of one cell and their influence on capacitor voltage, assuming the current direction in Fig. 1 is positive.

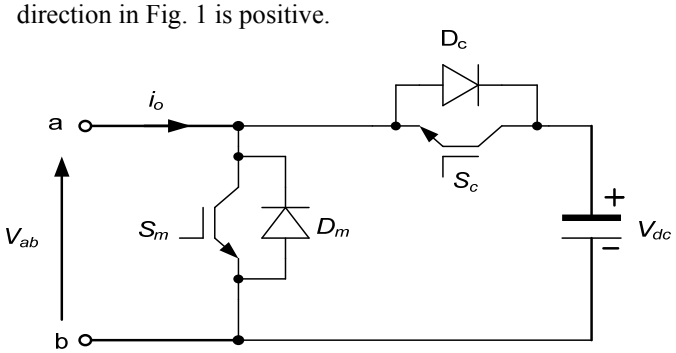


Fig. 1. Structure of one cell in a modular multilevel inverter

Table 1. Switch states of one cell

S_m	S_c	V_{ab}	Current direction	Power path	Capacitor state
ON	OFF	0	$i_o > 0$	S_m	unchanged
ON	OFF	0	$i_o < 0$	D_m	unchanged
OFF	ON	V_{dc}	$i_o > 0$	D_c	Charging
OFF	ON	V_{dc}	$i_o < 0$	S_c	Discharging

Fig. 2 shows one phase of a five-level modular inverter in which each voltage level can be synthesized by turning eight switching devices on in each instant. In each instant four switches must belong to the main group S_{a1} through S_{a8} and the remaining four must belong to the auxiliary switches S_{x1} through S_{x8}.

There are eight complementary switch pairs in each phase; turning one of the switch pairs on will prevent the other from being turned on. The eight complementary switches are (S_{a1}, S_{x1}) through (S_{a8}, S_{x8}). The voltage across each capacitor cell is $¼V_{dc}$ and the voltage stress in a switching device will be limited to one capacitor voltage. For an *n*-level inverter the voltage across each capacitor and switching device will be limited to $V_{dc}/(n-1)$ while the number of switching devices (e.g. IGBT plus free wheeling diode) required per phase is doubled compared to the diode clamped multilevel inverter. The number of capacitors required for a three-phase modular multilevel inverter is $6n-6$ ($2n-2$ per phase), while no clamping diodes are required.

To explain how the multilevel voltage waveform is synthesized in a five-level modular inverter, the supply midpoint is assumed as the output voltage reference; each capacitor in the five-level modular inverter circuit in Fig. 2 is fully charged to $¼V_{dc}$ and all the switching devices are ideal switches. There are 70 switch combinations to synthesize five-level voltage waveform between the output phase, a, and 0. Binary expression of the switch states will be used to explain how the voltage waveform is synthesized, for example, 1 represents the on-state and 0 represents the off-state.

- For voltage level $V_{a0}=½V_{dc}$, turn on all upper main switches (S_{a1}, S_{a2}, S_{a3} and S_{a4}) and all lower auxiliary switches (S_{x5}, S_{x6}, S_{x7} and S_{x8}). This switch combination can be represented in binary form as 00001111.
- For voltage level $V_{a0}=¼V_{dc}$, there are 16 switching states that produce $¼V_{dc}$. These switch states can be achieved by turning on three switches from the upper main group and one switch from the lower main group. Two of them are given below:
  - i) Turn on S_{a1}, S_{a2}, S_{a3} and S_{a5}.
  - ii) Turn on S_{a1}, S_{a3}, S_{a4} and S_{a8}.
- The voltage level $V_{a0}=0$, can be produced by 36 different switch combinations; these combinations can be achieved by turning on two switches from the upper main group and two from the lower main group.
- The voltage level $V_{a0}=-¼V_{dc}$, can be synthesized by 16 different switch combinations; these combinations can be achieved by turning on one switch from the upper main group of switches and three from the main switches.
- For voltage level $V_{a0}=-½V_{dc}$, turn on all upper auxiliary switches (S_{x1} through S_{x4}) and all lower main switches (S_{a5} and S_{a8}).

In order to maintain equal voltage stress across different switching devices the voltage across each cell capacitor must be maintained at $¼V_{dc.}$ therefore a capacitors voltage balancing method is required.

2.2 Pulse Width Modulation and Capacitors Voltage Balancing Method

In this paper, the sinusoidal pulse width modulation (SPWM) technique developed by Carrara is used to control each phase leg of a five-level modular inverter separately and to allow the line-to-line voltage to be developed implicitly [15]. As the modular multilevel inverter utilizes phase voltage redundancies to maintain the dc link capacitors voltage balance, the capacitors voltage balancing technique must be embedded within the modulator to facilitate the selection of the correct switch combinations that will lead to balanced dc link capacitors.

There are 70 switch combinations available in each phase of a five-level modular inverter. These switch combinations must be used properly to synthesized five levels waveform between a and 0, and to maintain the correct voltage across each capacitor in Fig. 2. To explain the effect of these switch combinations on voltage balancing of the dc link capacitors of a five-level modular inverter, the following switching combinations are considered:

The voltage levels $½V_{dc}$ and $-½V_{dc}$ can be synthesized by switch combinations 11110000 and 00001111 respectively. These two switching states do not affect the voltage balance of the dc link capacitors.

The 16 switch states that produce $¼V_{dc}$ voltage level will charge or discharge one capacitor from four upper capacitors and discharge or charge three capacitors from the lower four capacitors depending on the phase current direction. For example, when $i_a>0$, switch state 01111000 charges C_1 and discharges C_6, C_7 and C_8; and when $i_a<0$, discharges C_1 and charges C_6, C_7 and C_8.

The 16 switch states that produce voltage level $-¼V_{dc}$, will charge or discharge three capacitors from four upper capacitors and discharge or charge one capacitor from the lower four capacitors depending on the phase current direction. For example, switch state 00010111 charges C_1, C_2, C_3 and discharges C_5 when $i_a>0$, while discharges C_1, C_2, C_3 and charges C_5 when $i_a<0$.

The 36 switch combinations that produce zero voltage level will charge or discharge two capacitors from the upper group and two from the lower group, also, depending on the phase current direction. For example, when $i_a>0$, switching state 11000011 charges capacitors C_3, C_4 and discharges C_5 and C_6; when $i_a<0$ discharge C_3, C_4 and charges C_5 and C_6. Therefore, the cells capacitors can be balanced by proper selection of these switching combinations.

Based on these observations, the capacitors voltage balancing method for a five-level modular inverter is developed and implemented.

The capacitors balancing strategy for a modular inverter with more than five levels is similar to that of a five-level inverter, except that more sophisticated software overhead is needed to sort the capacitors according to their voltages and to determine which switch combinations need to be selected.

In the five-level case, capacitors C_1 through C_8 are used for one fourth of fundamental period, $¼T$, where T is fundamental period. Consider capacitor C_1 as an example. During the positive half of the load current, the capacitors C_1, C_2, C_3 and C_4 cannot be discharged and capacitors C_5, C_6, C_7 and C_8 cannot be charged, until the negative half of the load current. During this process if the sum of any four capacitor voltages in one of the phases exceed the total dc link voltage a circulating current will be created between this phase and the other phases. The circulating current is limited by inductance L in Fig. 2. This feature allows the modular converter to maintain a balanced dc link during unbalanced operation and a single-phase open-circuit fault in one of the phases. In order to maintain voltage balance of each capacitor cell, the average current drawn from each capacitor must be zero over one fundamental cycle.

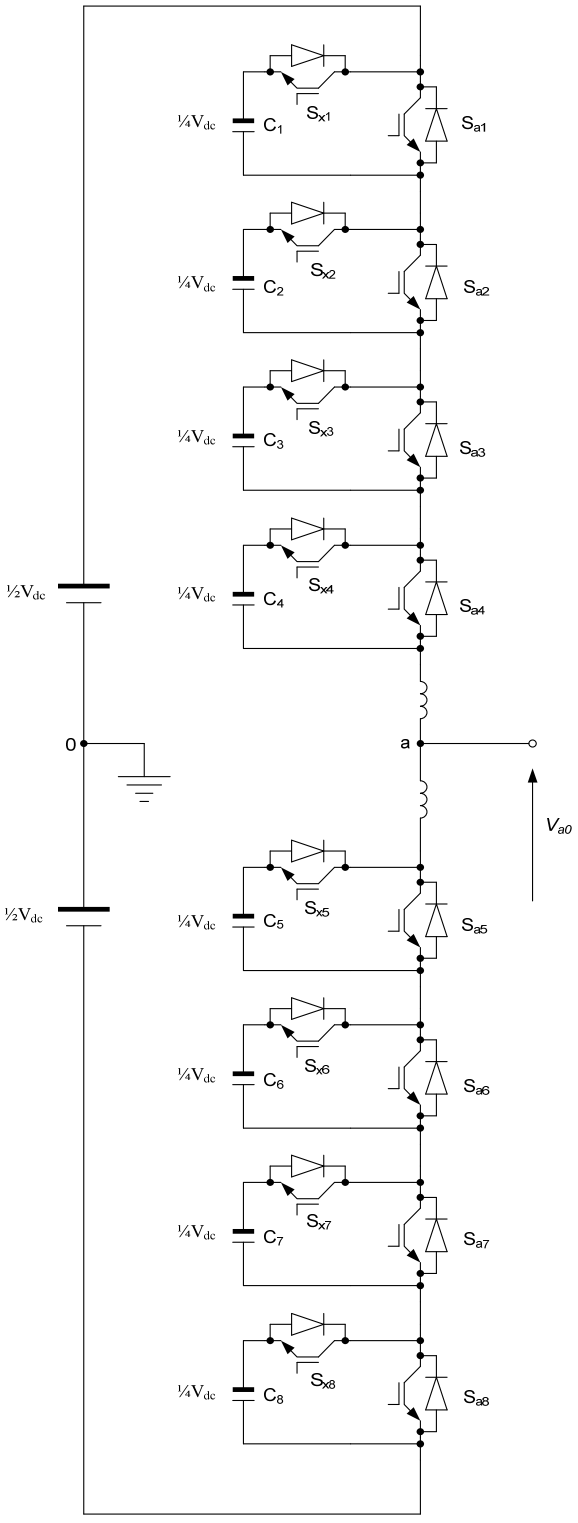


Fig. 2: One-phase of a five-level modular inverter.

Therefore, for an n-level inverter, each capacitor will be used only for *1/(n-1)* of the fundamental period, therefore with increased number of levels, each capacitor will be used for a short period of time, resulting in a significant reduction in capacitor size. Also, switching device

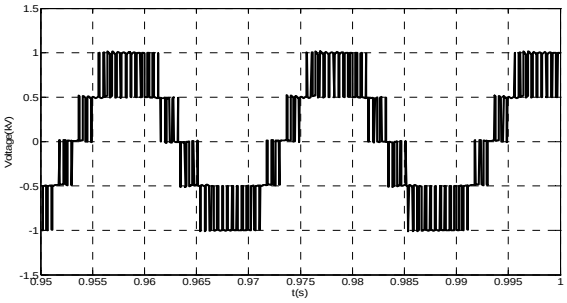
utilization is independent of its location in the circuit and of the modulation. In other words, each switching device is used for equal periods of time regardless of the modulation index, load power factor and its location in the circuit, as a result, the heat sinks will be rated the same for all switching devices.

3. Simulation Results

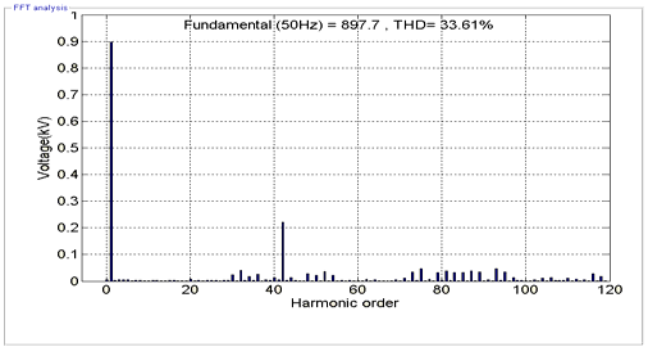
The results presented are obtained when a five-level modular inverter is simulated in Matlab-Simulink, with total dc rail voltage of 2kV and capacitor of 2200µF. Sinusoidal pulse width modulation with switching frequency of 2.1 kHz in conjunction with the presented capacitors voltage balancing method is used to control the switches of the five-level modular inverter in order to generate the desire output voltage and to force the capacitors voltages to follow their set points. Several scenarios have been considered to illustrate the suitability of the modular inverter with higher number of levels for medium and high voltage applications.

Fig. 3 shows the phase voltage and its spectrum, line-to-line voltage and its spectrum of five-level modular inverter operated with 0.9 modulation index and load power factor of 0.8. It can be noticed that the line-to-line voltage total harmonic distortion (THD) is half of that of the phase voltage; this is due to placement of significant amount of harmonic energy at the first carrier component of the phase voltage which is canceled in the line-to-line voltage as shown in Figs. 3b and 3d. The harmonics distribution along the spectrums of the phase and line-to-line voltages of the five-level modular inverter with PD (phase disposition) carriers is identical to that of a five-level diode clamped inverter with PD carriers. Also, it can be noticed that the voltage balance of the dc link capacitors remains firm.

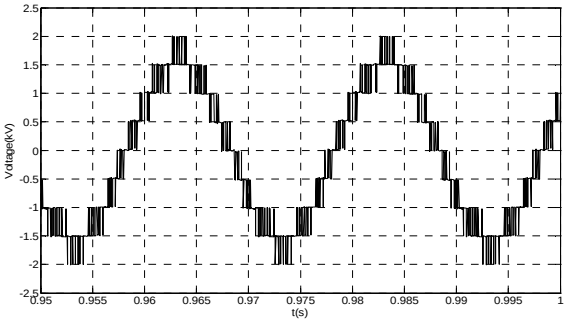
Figs. 3a and 3c show the principle of minimum switching losses (switching of one voltage level at each instant) is maintained, resulting in low voltage stress of switching devices and dv/dt.



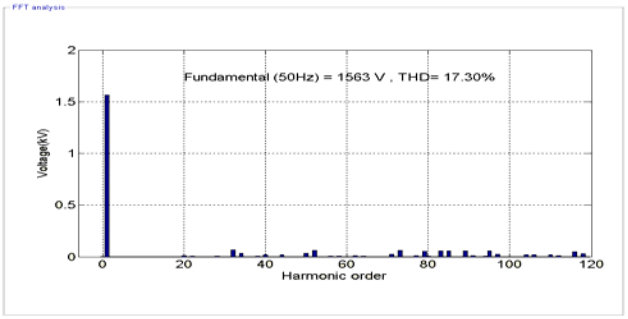
(a) Phase voltage referred to ground 0



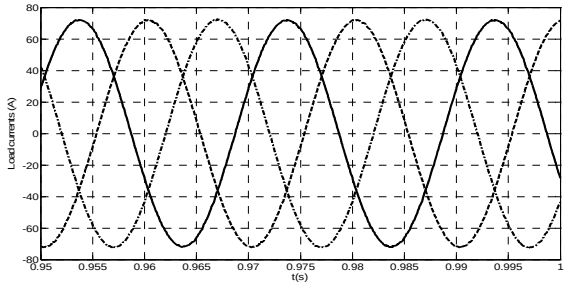
(b) Phase voltage spectrum



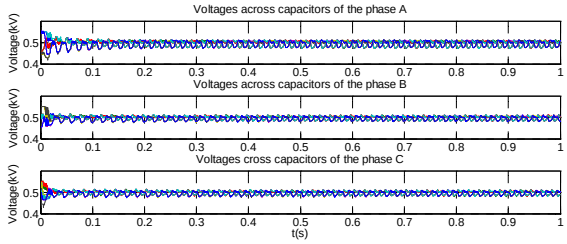
(c) Line-to-line voltage



(d) Line-to-line voltage spectrum



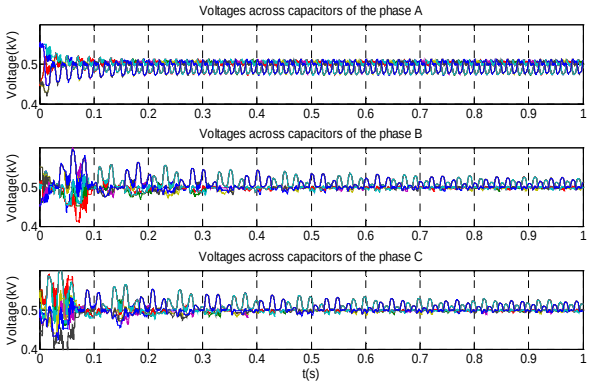
(e) Load current



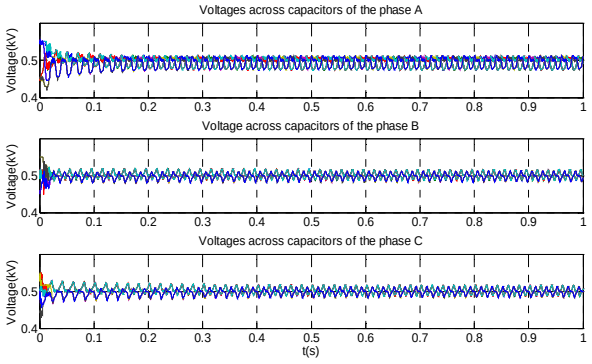
(f) Voltage across dc link capacitors

Fig. 3: Voltage and current waveforms of a five-level modular inverter when modulation index m=0.9 and load power factor pf=0.8 lagging.

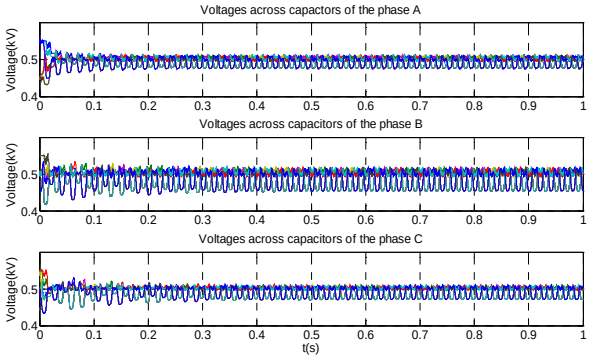
To show the effect of the modulation index and the load power factor on voltage balancing of the dc link capacitors, several operating conditions are considered, including operation with different modulation indices and load power factors.



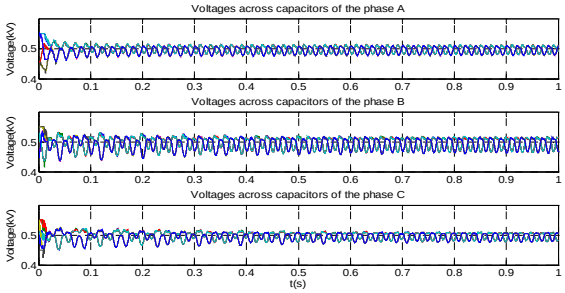
(a) Modulation index m=0.9 and zero power factor



(b) Modulation index m=0.9 and unity power factor



(c) Modulation index m=1 and load power factor pf=0.8 lagging

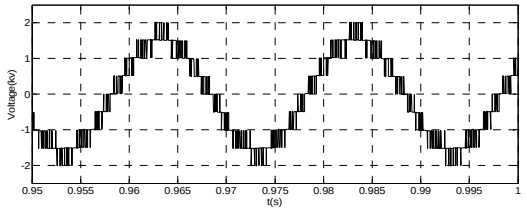


(d) Modulation index m=0.5 and load power factor pf=0.8 leading

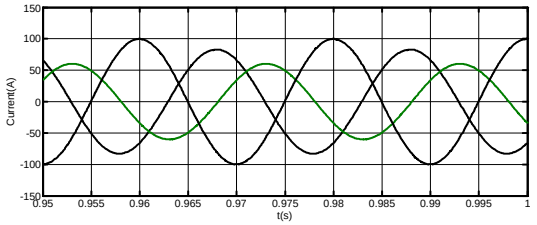
Fig. 4: Effect of load power factor and modulation index on the dc link capacitors voltage balance

The results in Fig. 4 demonstrate that the voltage balance of the dc link capacitors of a five-level modular inverter is achievable over the full linear range of modulation index and load power factor (lagging or leading).

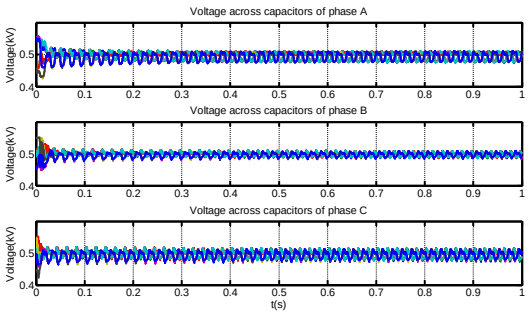
Fig. 5 shows that the five-level modular inverters are capable of operating continuously under unbalanced conditions without increasing the risk of device failures due to increased voltage stresses as a result of dc link voltage imbalance. Also, it can be noticed that despite the unbalanced operating condition, the output voltage remained balanced and undistorted. This feature may allow modular multilevel inverters with more than three-levels to dominate inverters' applications in power systems.



(a) Line-to-line voltage



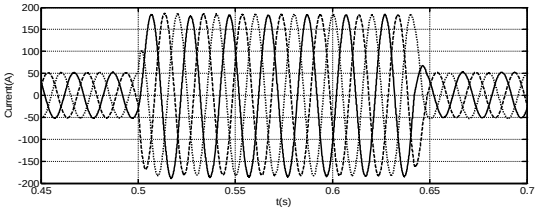
(b) Load current



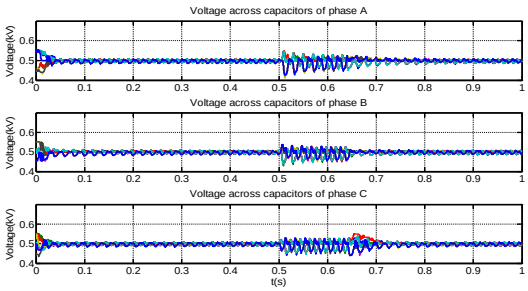
(c) Voltage across the dc link capacitors

Fig. 5: Effect of continuous operation with unbalanced load (R_a=10 Ω, X_{La}=7.5 Ω, R_b=1.5×R_a, X_{Lb}=1.5×X_{La}, R_c=0.5×R_a and X_{Lc}=0.5×X_{La})

The results in Fig. 6 are obtained when a five-level modular inverters is subjected to a three-phase short circuit with duration of 7 cycles at its terminal through fault impedance of (4+j3) Ω. It can be seen that the voltage balance of the dc link capacitors are maintained



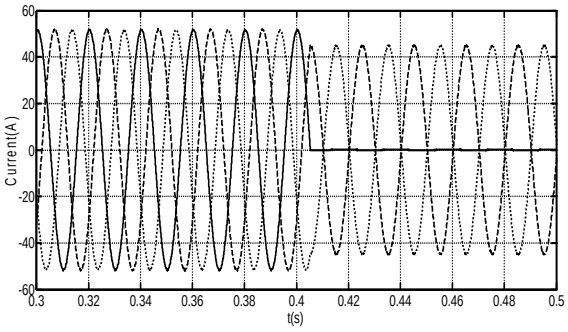
(a) Load current during a three-phase short circuit



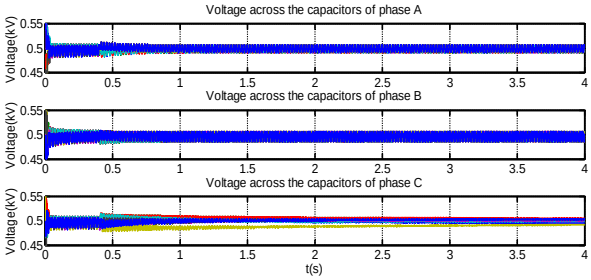
(b) Voltage across the dc link capacitors of the five-level modular inverter during a three-phase short circuit.

Fig. 6: Load current and capacitor voltage waveforms of a five-level modular inverter during a three-phase short circuit fault.

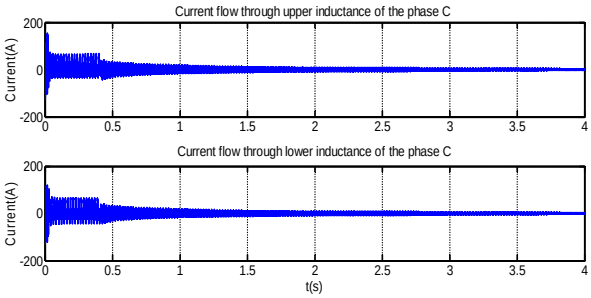
Fig. 7 shows the results obtained when a five-level modular inverter is subjected to a single-phase open circuit fault at phase C. The results demonstrate the ability of a five-level modular inverter to survive the worse type of asymmetrical faults that most of the established conventional multilevel inverters such diode clamped inverter (three-level or five-level) which depend on space vector with the help of line-to-line redundant states will not survive (because under such operating conditions space modulation becomes invalid). It can be noticed from Fig. 7c, that there are circulating currents from the healthy phases (A and B) flowing through the upper and lower inductances of the faulty phase (C) to redistribute the voltage correctly across the capacitors of the phase C.



(a) Load current when phase C is subjected to open circuit



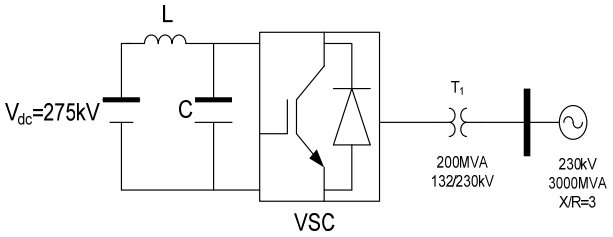
(b) Voltage across the capacitors of the three-phase of a five-level modular inverter



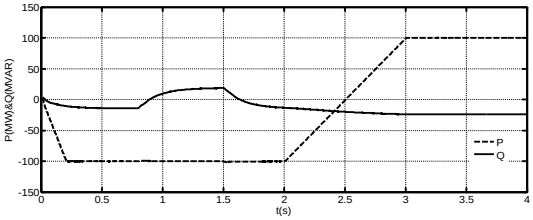
(c) Current flow in the upper and lower inductance

Fig. 7: Load current, capacitor voltages and inductor current waveforms during single-phase open circuit fault at phase C.

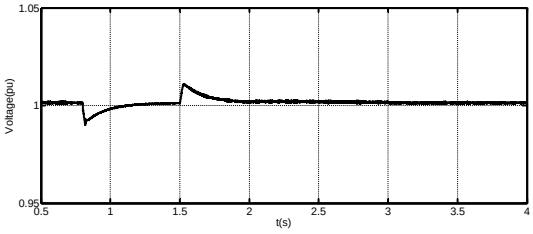
For the grid connected inverter scenario, a 275kV, 200MVA storage system with bidirectional power flow capability, Fig. 8a, is considered. The VSC is represented by a three-phase five-level modular inverter controlled using SPWM with switching frequency of 2.1 kHz. The inductance L is used to allow the dc link voltage to increase or decrease according to the power flow direction. During the starting an active power command is given to the VSC to ramp up the imported power from the grid from 0 to -100MW within the first 200ms. To demonstrate the reactive power capability of a modular inverter, a load of 50MVA with power factor of 0.8 lagging is switched in and out at times t=0.5s and 1.5s respectively. To demonstrate the robustness of the capacitor voltage balancing method and control flexibility of the modular inverter, another active power command is given at time t=2s to reverse power from -100MW to 100MW within 1s. The results in Fig. 8 show the key waveforms obtained. It can be observed that the voltage balance of the dc capacitors remained firm during the power reversal and the voltage across the dc link capacitors are moving up and down according to the ac power flow direction in the ac side.



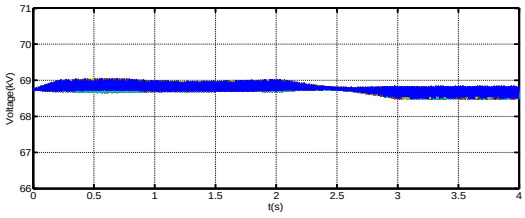
(a) Storage system connected to the grid using five-level modular inverter



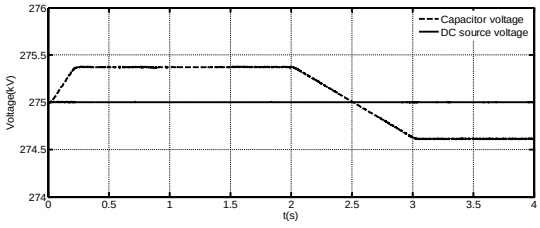
(b) Active and reactive power released or absorbed by inverter



(c)Voltage magnitude at bus B1



(d)Voltage across DC link capacitors of phase A



(e) DC link Voltage during power reversal.

Fig. 8: Schematic diagram and key waveforms obtained

4. Conclusion

The paper described the operational principle and theoretical basis of the dc link capacitors voltage balancing technique of the five-level modular inverters. It has been found that the modular multilevel inverters with capacitors voltage balancing technique using carrier based PWM perform better than conventional multilevel inverters in the following sense:

1. Capacitors voltage balance can be attained for any number of levels.
2. Capacitors voltage balance is independent of load power factor and modulation.
3. Extremely low total harmonic distortion can be achieved if a large number of levels are used.
4. Voltage stress on switching devices is limited to one capacitor voltage regardless of operating conditions.
5. It has phase voltage redundancy which makes capacitors balancing strategy relative easy and robust compared to conventional multilevel inverters with only line-to-line redundancy.
6. Despite significant increase in number of switching devices and capacitors when the number of levels increases, the complexity of modulation and capacitor balancing techniques remain simple.

References

[1] A. Nabae et al., "A New Neutral-Point-Clamped PWM Inverter," IEEE Trans. Industry Applications, Vol. 1A-17, No. 5, Sept/Oct. 1981, pp. 518-523.

[2] J.S. Lai and F.Z. Peng, "Multilevel Converters-A new breed of power electronic converters,"IEEE Trans. Industry Applications, Vol. 32, No. 3, May/June 1996, pp. 509-517.

[3] G. Sinha and T. A. Lipo, "A Four –Level Rectifier-Inverter System for Drive Applications," IEEE Industry Applications Magazine, January/February 1998, pp. 66-74.

[4] J. Pou et al., "Voltage balance limits in four level diode clamped converter with passive front ends," IEEE Trans. Industrial Electronics, Vol. 52, No. 1, February 2005, pp.190-196.

[5] M. Saeedifard et al., "Analysis and control of DC-capacitor-voltage drift phenomenon of a passive front-ends Five-level converter," IEEE Trans. Industrial Electronics, Vol. 54, No. 6, Dec. 2007, pp. 3255-3266.

[6] Pou et al., "Effects of Imbalances and Nonlinear Loads on the Voltage Balance of a Neutral Point-Clamped Inverter," IEEE Trans., Power Electronics, Vol.20, Issue 1, 2005, pp. 123-131.

[7] Maryam. S et al., "Analysis and Control of DC Capacitors-Voltage-Drift Phenomenon of a Passive Front-End Five-Level Converter," IEEE Trans. Industrial Electronics, Vol. 54, No. 6, Dec. 2007, pp.3255-3206.

[8] Maryam. S et al., "A Space Vector Modulation Strategy for a Back-to-Back Five-Level HVDC Converter System," Accepted in IEEE Industrial Electronics Journal.

[9] K. Yamanaka et al., "A Novel Neutral Point Potential Stabilization Technique Using the Information of Output Current Polarities and Voltage vector," IEEE Trans. Industry Applications, Vol. 38, No. 6, Nov/Dec. 2002, pp. 1572-1580.

[10] C. Newton and M. Sumner, “Multilevel Converters: A Real Solution to Medium/High-Voltage Drives,” IEE Power Engineering Journal, Vol. 12, Issue 1, February 1998, pp. 21 26.
[11] C. Newton and M. Sumner, “Novel technique for maintaining balanced internal DC link voltages in diode clamped five-level inverters,” IEE Proc. Electrical Power Applications, Vol. 146, No. 3, May 1999, pp.341-349.
[12] V. Jouanne et al., “A Multilevel Inverter Aproach Providing DC-Link Balancing, Ride-Through Enhancement, and Common-Mode Voltage Elimination,” IEEE Trans. Industrial Electronics, Vol. 49, No. 4, August 2002, pp. 739-745.
[13] A. Lesnicar and R. Marquardt, “An Innovative Modular Multilevel Converter Topology Suitable for Wide Power Range,” IEEE Power Tech. Conference, Vol. 3, Bologna, Italy, June 23-26.
[14] M. Hagiwara, and H. Akagi, “Control and Experiment of Modular Multilevel Converters,” IEEE Power Electronic Specialist Conference, 15-19 June 2008, pp. 154-161.
[15] G. Carrara et al., “A new multilevel PWM method: A theoretical Analysis,” IEEE Trans. Power Electronics, Vol. 7, No. 3, July 1992, pp. 497-505.