Proceedings of the Ninth IASTED European Conference
Power and Energy Systems (EuroPES 2009)
September 7 - 9, 2009 Palma de Mallorca, Spain

EMBEDDING HIGH-SPEED POWER ELECTRONICS SIMULATIONS IN REAL-TIME POWER SYSTEM SIMULATIONS

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ABSTRACT
Advances in power electronics have revolutionized the design of electrical power systems, particularly in modern applications such as the connection of renewable power sources (e.g. wind, solar) to power grids, power systems for all-electric ships etc. These changes have generated a need for advances in the simulation techniques for such systems, particularly for real-time simulation. Simulation of power converters with controllers switching at kHz frequencies requires frame times that are much shorter than the traditional 50 μsec frame. In addition to the challenge of achieving accurate real-time simulations with frame times as short as 1 μsec or even less, it is necessary to integrate these high-speed components with the real-time simulation of the rest of the system. One approach is to design a simulator that combines high-speed real-time platforms with a more conventional real-time simulation system in a distributed multi-rate configuration.

KEY WORDS
Simulation, real-time, multi-rate, power systems.

1. Introduction

Improvements in power electronic techniques, particularly in allowing higher switching frequencies to reduce lower-order harmonics, have necessitated new developments in simulation techniques for power electronic systems. This is especially true in the case of real-time simulation, for which traditional frame times must be greatly reduced to avoid serious errors in the timing of switch operation. Techniques are described which have reduced typical frame times from 50 μsec to less than 1 μsec. This performance requires special hardware and software techniques and raises questions as to how these high-speed elements can be embedded in a complete power system simulation in which many of the components can be simulated using much longer frame times. An approach based on multi-rate real-time simulation is described and some suggestions made regarding possible architectures for a high-speed, real-time, distributed, multi-rate (HRDM) simulator.

2. Background

The use of computers to simulate electrical power systems has a long history, almost as long as the history of computing itself. Two of the authors were involved in early studies of simulating power converters in high voltage direct current (HVDC) systems [1]. A key contribution to the simulation of a.c. systems was made by Dommel and coworkers in the early 1970s [2] with a computational approach that resulted in the development of the Electromagnetic Transients Program (EMTP) [3,4]. EMTP has been a mainstay of power system simulation ever since. The use of one of the many versions of EMTP with an integration step-size of 50 μsec became a de facto standard for power system simulation. Improvements in solid-state switch devices led to advances in the use of power electronics in many power systems applications. It became necessary to revisit the question of suitable integration time steps for power system simulation as 50 μsec became too long to maintain accuracy in the face of the increased switching frequencies used in power converters. When the simulation includes switching operations, timing errors are introduced whenever a switching event fails to coincide in time with the end of an integration step. When real-time operation is not required, algorithms can be used that vary the step size and adjust it to ensure that timing errors are kept within a user-specified tolerance [5]. Fixed-step codes such as EMTP have no problem adapting to shorter integration step sizes although execution time increases as step size becomes smaller. Real-time simulation, which is necessary when hardware, software or human operators interact with the simulation, presents a more difficult problem. Step adjustment algorithms are inappropriate and fixed-step algorithms must be used, but the shorter the step-size, the less time is available for updating the solution.

Available commercial real-time simulation systems offer frame times as low as about 10 μsec. These systems are usually based on a real-time implementation of the Linux operating system and operating system jitter limits the lowest available frame times. Special techniques are

needed to achieve the 1-μsec and shorter frame-times needed for modern power electronic systems.

A further problem is that, given a high-speed real-time simulation platform capable of these speeds, the simulation of the rest of the system still needs to be performed on more conventional platforms and at rates more appropriate to the dynamic behaviour of these components. Multi-rate simulation techniques are well known and have been used for many years, but they need to be adapted to work with high-speed real-time techniques. There is therefore a need for an integrated high-speed, real-time, distributed, multi-rate (HRDM) simulator that can effectively simulate all parts of the target system.

Systems are available that will handle such broad-spectrum real-time power system simulations. RTDS of Manitoba, Canada supplies multiple-processor systems with customized components designed specifically for power system simulation [6]. These systems offer high-speed processing units capable of 2-μsec frames. Systems of this kind are, however, expensive (hundreds of thousands of US dollars). The aim of the Chico research is to design systems with capable of sub-microsecond frame time using off-the-shelf components and costing less than $100K. The paper describes progress towards this goal.

3. High-Speed Real-Time Techniques

Against this background, the initial research effort [7-9] investigated available off-the-shelf components and systems, seeking a way to achieve cost-effective, real-time simulations with frame times of 10 μsec or less. The initial choice fell upon an array of 4 digital signal processors (DSPs) mounted on a board that was inserted into the PCI bus of a conventional desktop computer. Boards of this type are available as off-the-shelf components from several manufacturers for a few thousand dollars.

A benchmark application was selected for comparing the performance of different programming methods. The benchmark was based on a 3-phase, back-to-back, a.c. to d.c. to a.c. system with 2-level 6-pulse voltage-sourced converters, harmonic filtering, and pulse-width modulation controllers offering voltage, current, and active and reactive power control. The math model consisted of 23 first-order, ordinary, linear differential equations plus switching logic, sine-triangular wave comparisons for the PWM controllers, and PI control algorithms. Initially, simple first-order Euler integration was used to solve the differential equations. The Euler method was selected because it involves the minimum of calculation to advance the solution of the differential equations in time, and it was not expected that truncation errors would cause problems because the integration step size was required to be very short to minimize timing errors.

To simplify the program coding and keep execution time to a minimum, the integration algorithm was combined with the differential equations to form a set of difference equations before coding. The difference equations were then programmed in C and compiled to produce executable code. The simulation was separated into four parts, each part being implemented on one of the four processors. The partitioning scheme, which was based on a logical separation of the physical system into its main components, worked well and was maintained with minor changes throughout the project. It involved committing one processor to each of the two converters and associated circuitry, one processor to the two sets of controllers and the fourth processor to synchronization and data transfer functions.

At first the simulation suffered from two major problems. One was that the C-compilers provided with the processors proved very inefficient because they did not take advantage of the high degree of parallelism built into the DSPs. To achieve acceptable performance this necessitated considerable hand coding, which is both time-consuming and error-prone. Fortunately, this problem disappeared with later versions of the compiler which proved capable of generating highly efficient code.

The second problem was that the simulation was unstable with some values of the circuit parameters. Euler integration, in common with all explicit, single-step, numerical integration algorithms can produce unstable solutions if the step size is too large compared to the smallest eigenvalue of the set of differential equations. For Euler integration the solution will be unstable if

$$h > 2\lambda$$

where h is the integration step size and λ is the smallest eigenvalue. Stability analysis showed that the simulation would become unstable with parameter values that could occur in practice and execution of the program confirmed the results of the analysis.

3.1 Improved Integration Algorithms

A more suitable integration algorithm was sought that would combine improved stability characteristics with low computational cost. Second-order Runge Kutta is a possibility but it involves twice the computation and offers only a modest improvement in stability. Since the circuit equations in the systems of interest are linear, methods based on linear state transition theory were investigated. This approach produces a solution, under certain assumptions, that is guaranteed stable if the system of differential equations is stable. It is, however, based on the evaluation of the sums of infinite series. Truncating these series is possible, although numerical

stability is no longer guaranteed. Extensive investigation and analysis showed that a state transition approach based on truncating the two infinite series to three and two terms respectively works well. This is referred to as the ST(3,2) method. It has been used extensively in the research. It has been compared in performance and stability tests with several other candidate methods including 2^{nd}-order Adams-Bashforth and implicit trapezoidal (the method used by EMTP) and in general it demonstrates superior performance in these tests [10].

Using the latest DSPs with their efficient new compilers, the ST(3,2) integration algorithm, and with carefully designed I/O processes, the minimum integration step-size for the 6-pulse back-to-back benchmark was reduced to 2.02 μsec.

3.2 Graphical User Interface

The Virtual Test Bed (VTB), developed at the University of South Carolina [11], was used to provide a user interface. The VTB is a complete simulation system in its own right, but in this case it was used simply to provide a means of setting up the simulation, entering parameters, controlling the execution of the simulation and graphical display of the results. Because the rate at which data is produced by a real-time simulation running at a frame rate of 500 kHz is too high for the graphics routines to handle, short bursts of data were buffered and displayed, representing time slices of data output. For test purposes the execution of the simulation could be delayed to allow display of complete waveforms.

3.3 Field Programmable Gate Arrays (FPGAs)

As stated earlier, a frame time of a little more than 2 μsec was achieved using an array of 4 DSPs. At this stage a review of possible future progress concluded that no further reductions were likely using this type of processor, either from further improvements in coding or from the availability of more powerful processors.

It was therefore decided to investigate the use of field-programmable gate arrays (FPGAs). These devices offer a different challenge to designers who must configure the parallel functional units of the FPGA in a way that performs the necessary computation. Two programming approaches are available. Hardware description languages such as VHDL can be used as in place of C programming. A more direct approach is available uses a Simulink blockset that allows the designer to compose a graphical layout of FPGA functional units to solve the model equations. Because the difference-equation model for these power electronic applications consists mainly of calculations of sums of products, this method was chosen. The designer still has to organize the calculations in a sequential manner, since there are insufficient multiplier and adder units to perform all the calculation in parallel. It is, therefore, necessary to use multiplexers to select different data sets at the inputs to the arithmetic units.

Using this approach the same 6-pulse benchmark has been executed with a frame time of 400 nsec. Results compare closely with those obtained from both DSP and PC non-real-time implementations [12]

There are some issues with FPGAs that don't arise with other types of processor. FPGA computation is not floating point. The FPGA uses fixed-point arithmetic and it may be necessary to scale the system variables to avoid round-off error. Because the applications used so far use normalized variables, this has not so far been a problem.

4. Multi-Rate Simulation

In order to carry out a real-time simulation of a complete power-system application, for example the integrated power system for an electric ship, it is necessary to combine high-speed and lower-speed elements. It is neither necessary nor desirable to execute the entire simulation at the fast frame rate of the high-speed components, and a multi-rate approach is favoured in which different parts of the simulation execute with different frame rates, selected to match the dynamic behaviour of that particular part of the system. Care must be taken in partitioning the system and selecting frame rates to ensure that the resulting simulation is stable and accurate. In particular it may be necessary to add anti-aliasing filters between faster and slower components to prevent aliasing occurring when a variable with higher frequency components may be sampled at too slow a rate at the input to a segment with a lower frame rate.

The multi-rate approach was tested initially using simple multi-loop electrical circuits. A method of performing stability analysis of bi-rate systems was developed and tested using these circuits, but a more realistic application was clearly needed to act as a multi-rate benchmark.

4.1 Multi-Rate Benchmark: Unmanned Underwater Vehicle (UUV)

The Chico team collaborated with researchers at the University of South Carolina and the University of Glasgow to create a more realistic multi-rate application with a high-speed component that could be used as a multi-rate benchmark [12-14]. The chosen application was an unmanned underwater vehicle (UUV). The main components of the UUV are a battery, d.c. to a.c. converter with PWM controller, harmonic filter, electric motor, drive shaft and thrusters, and a 6-degree of freedom model of the vessel with control planes. The converter and controller form the high-speed component, electric motor drive the medium-speed and the battery, and ship the low-speed elements of the multi-rate simulation.

The UUV multi-rate simulation was first implemented as a non-real time program, and this presented several challenges. The different models that made up the complete simulation originated from different research groups using different programming tools. The battery and electric motor were created from VTB internal models using the resistive companion matrix approach (similar to EMTP) to solve differential equations, the ship model was originally in Matlab using 4^{th}-order Runge Kutta and was reprogrammed in C, and the converter and controller used the high-speed ST(3,2) method.

As with the 6-pulse high-speed benchmark, VTB provided the user interface for the UUV program, and in addition to graphical outputs the 3-D animation capability of the VTB graphics system was used to provide a 3-dimensional view of the vessel motion including rotation of the thrusters and movements of the control planes.

The UUV benchmark has proved to be a useful application with which to investigate multi-rate methods. It has been implemented in non-real-time on both Windows and Macintosh computers and with reasonable frame rates executes close to or faster than real-time. By contrast, when executed using the shortest (high-speed) frame time of 2 μsec for all parts of the simulation it runs several hundred times slower than real time with little apparent change in results demonstrating the value of the multi-rate approach.

The next step is to implement the UUV benchmark as a true high-speed, real-time, distributed multi-rate (HRDM) simulation.

4.2 HRDM Simulator

It is not normally cost-effective to implement the entire simulation on the high-speed platforms. It is therefore likely that the complete simulator will consist of one or more FPGA or other high-speed elements combined with a more conventional real-time simulation platform. In order to handle medium-speed components (frame times down to about 10 μsec) this will probably consist of a real-time Linux system.

A minimal HRDM simulator would consist of a high-speed (DSP or FPGA) processor, a real-time Linux system and a hardware-in-the-loop interface. Because the VTB is a key part of the UUV simulation, a Windows platform is also required. Windows is not classed as a real-time operating system because system routines have a higher priority than user applications leading to large timing uncertainties when executing time-critical code. However, as long as allowance is made for these long latencies, some slow frame rate components could possibly be executed in the Windows system. Preliminary measurements suggest that frame rates in the tens of microseconds range might be feasible.

Because of the reliance on VTB the Chico HRDM simulator will consist of high-speed (FPGA), medium-speed (real-time Linux), and low-speed (Windows) components with the user interface (VTB) on the Windows system.

One of the major remaining challenges to completing the simulator is the design of the interface between the separate parts of the system. Current work is aimed at customising an Ethernet-based system bus to achieve the required performance. Transmission bandwidth is, in this case, less of an issue than latencies. It is inevitable that when data is transmitted from one part of the system to another, it will be out of date by the time it is received. It is important that these time delays are minimised and that where necessary compensation techniques are used to counteract their effect.

4.3 Interim Real-Time Simulation Results

The design and construction of the Chico HRDM simulator is ongoing. It is only possible at this stage to give partial experimental results that give some indication of the likely performance to be expected from the completed simulator.

First there is a lot of data about the performance of isolated high-speed power electronics simulations. Much of the initial research was focused on this aspect since it was seen as the key to achieving successful real-time simulation of modern power systems. The most frequently used example at Chico is the 6-pulse back-to-back benchmark described in Section 2. As mentioned earlier, this has been run in hard real-time on both DSP and FPGA processors and has achieved minimum frame times of 2.02 μsec and 400 nsec respectively. This provides a firm basis on which the research can proceed to multi-rate distributed simulation.

The second step was the development of the UUV multi-rate benchmark. The initial implementation was made on conventional PCs using multi-rate algorithms. Although this implementation could not be run in real-time, it demonstrated the power and effectiveness of the multi-rate approach which, with careful programming and algorithm selection, was capable of running slightly faster than real time on a conventional laptop computer. The high-speed (converter and controller) part of this simulation has been run separately, in real-time, on an FPGA and the rest of the system has been ported to an ADI rtX real-time Linux system.

The current status of this development is that parts of the system have been tested on interconnected pairs of systems. The rtX (medium speed) has been coupled to the PC (VTB user interface and slow speed); the FPGA (high-speed) has been interfaced to the rtX system; and a complete multi-rate distributed, but non-real-time implementation involving 3 PCs has also been tested.

These various configurations allow testing of different aspects of the behaviour of the completed system. The key outstanding unknowns concern the achievable bandwidth and latency of transferring data between platforms and its effect on accuracy of the complete simulation. This is particularly critical for the high-speed elements. One thing is certain and that is that any data transmitted from one platform to another in a real-time simulation will be out of date by the time it is received. Techniques are available to compensate for these errors either by sending predicted future data values, or by correction of received data.

Future plans involve the testing of each of the suggested configurations with a comprehensive evaluation of each with respect to choice of algorithms, frame rates, interface performance, and potential cost.

5. Conclusion

Power electronics is playing an ever increasing role in the design of advanced power systems. This is particularly true for sources of renewable energy such as wind and solar. Currently available real-time simulation techniques are not capable of achieving the performance required for many of these systems. Progress in high-speed real-time and multi-rate distributed techniques offers promise in meeting the future needs of power system simulation.

Acknowledgements

The authors acknowledge contributions by Dr. Euan McGookin and Professor David Murray-Smith of the University of Glasgow and by Professor Roger Dougal and the VTB team at the University of South Carolina. They also acknowledge financial support from the US Office of Naval Research.

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